



Patent Application
Attorney Docket No.: 57941.000063
Client Reference No.: RA001.2003.2.C.US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: :
: :
Michael FARMWALD et al. :
: Group Art Unit: Unassigned
Appln. No.: 10/716,596 :
: Examiner: Unassigned
Filed: November 20, 2003 :
: :
For: INTEGRATED CIRCUIT I/O USING :
A HIGH PERFORMANCE BUS :
INTERFACE :

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with the duty under 37 C.F.R. § 1.56 of each individual associated with the filing and prosecution of the above-identified patent application (hereinafter, "associated individuals") to disclose all information known to that individual to be material to patentability, Applicant(s) hereby submits attached Form PTO-1449 (modified) listing cited references. This submission is made in accordance with 37 C.F.R. §§ 1.97 and 1.98 and § 609 of the Manual of Patent Examining Procedure.

The cited references, while believed to be of some relevance, are not necessarily considered to teach or suggest any aspect of the invention described and claimed in the above-

identified patent application. Applicant(s) hereby expressly reserves the right to swear behind the effective dates of any of the cited references. Applicant(s) further reserves the right to question the relevance, materiality, and/or prior art status of any of the cited references in whole, in part, or in combination, subsequent to the filing of this information disclosure statement. This information disclosure statement is also not to be construed as a representation that a search has, or has not, been conducted or that no better art exists. Rather, this information disclosure statement discloses only the best references of which the associated individuals are aware.

The Examiner is respectfully requested to consider each of the cited references, to indicate such consideration by initialing in the space provided next to each cited reference on the enclosed Form PTO-1449 (modified), to sign the initialed Form PTO-1449 (modified), and to return a copy of the same with the next communication to the Applicant(s).

Since copies of the cited references were previously submitted in prior U.S. Patent Application No. 10/037,171, copies of the cited references are not being submitted herewith. However, copies will be forwarded at the request of the Examiner.

In accordance with 37 CFR § 1.97(b), this information disclosure statement is being filed (i) within three months of the filing date of the above-identified patent application; (ii) within three months of the date upon which the above-identified patent application entered the national stage as set forth in 37 CFR § 1.491; or (iii) before the mailing date of a first Office Action on the merit for the above-identified patent application. Accordingly, no statement or fee is required.

Please charge any shortage in fees due in connection with the filing of this communication to Deposit Account No. 50-0206, and please credit any excess fees to such deposit account.

Respectfully submitted,

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Date: February 6, 2004

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PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. 57941.000063	SERIAL NUMBER 10/716,596
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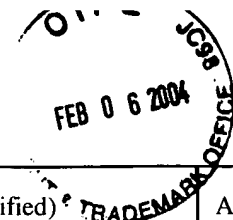
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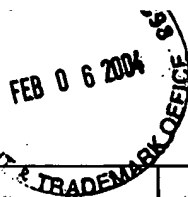
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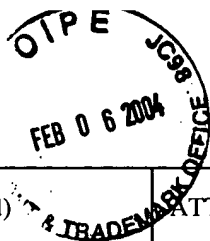
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	APPLICANT(S) MICHAEL FARMWALD ET AL.	
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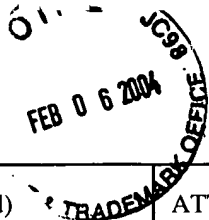
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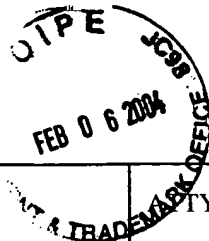
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